distributes this signal to all data channels within the DSC Module. The BIST block provides a means for testing critical functionality of the entire DSC Module and reporting self-test status. The utility block provides logical functions to coordinate the interface between a cold training sequence, warm training sequence, and DSC and core logic and the data FIFO read pointer control across the bundle.

Each data channel of a DSC Module is preferably comprised of three sub-blocks, including a data channel front end, data FIFO, and utility block. The data channel front-end block functions to phase-correct the data and clock signal edges during the phase correction sub-sequence of the cold or warm training sequences. Once phase correction has been completed, the data-recovery link clock signal from the clock channel is employed to sample the phase-corrected data. The data FIFO block receives positive and negative phase-aligned data from the data channel front end and stores this data in a FIFO framed on the prescribed byte boundaries. The data FIFO block is also used to detect commands to initiate a warm training sequence and the SSM byte used to initialize the write pointer frame counter and start the data FIFO read pointers in the bundle for both cold training sequence and warm ~~warn~~ training sequence operations. The utility block of the data channel performs two primary functions, namely, 1) data FIFO read pointer control and coordination and 2) diagnostic register control and interface.

The Bundle Interface Module (BIM) distributes, re-times, and logically combines broadcast signals between all DSC Modules in the bundle. The BIM also functions to combine broadcast module status signals from all DSC Modules within the bundle to interface to the core logic.